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InP—An Assessment of United States Activities

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The activities toward developing a viable InP technology in the United States are quite recent. However, they now encompass a broad spectrum ranging from compounding through epitaxial deposition of ternary and quaternary alloys to device evaluation. Undoped semicrystalline InP has been prepared with mobilities of greater than 5400 and 90,000 $cm^2/volt$ sec at 300°K and 77°K respectively. Semiinsulating single crystals have been made with resistivities in excess of 10^7 ohm-cm having iron doping concentrations →

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in the low 10^{16} atoms/cm^3 range. Liquid phase epitaxial InP films grown directly on semiinsulating substrates have yielded carrier concentrations of 1×10^{15} and mobilities of over 70,000 at 77°K. This review will discuss questions concerning the material aspects, the band structure, the transport and chemical properties, and the devices of indium phosphide in an effort to resolve the primary question — is there a future for indium phosphide in microwave and millimeter wave devices and systems.

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InP — An Assessment of United States Activities

1. INTRODUCTION

This report will assess activities within the United States directed toward the development of an InP based microwave and millimeter wave technology. The background and status of the materials and device work on this III-V compound through June 1973 has been covered in a previous communication (Lile[1]).

Questions concerning the material aspects, band structure, transport and chemical properties, and device status as well as other pertinent areas will also be discussed to help resolve the primary question – is there a future for indium phosphide in microwave and millimeter wave devices and systems? After a detailed discussion of InP material activities in the United States, the justification for the work will be outlined based on the electrical and physical parameters of InP and the current status of indium phosphide devices. In order to fully explain and evaluate the potential of InP for microwave and millimeter wave devices, this report will review United States as well as other sources. At the outset, it must be stated that the microwave effort in the United States is very limited with the Department of Defense funding most of the programs at in-house laboratories and on contract to industry and universities.

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Due to the large number of references (145) in this report, the references will not be footnoted. See references, page 49.

The motivating drives within the semiconductor device industry are higher efficiency, speed, and power, and lower, cost, noise, and size. It was the first of these, in 1970, that prompted Hilsum and Rees[2] to propose that semiconducting InP might offer advantages over, for example, GaAs in the area of Gunn device applications. This proposal and the subsequent work that ensued was as a result primarily addressed to the Transferred Electron Device (TED). Since then subsequent materials developments have encouraged researchers to consider the application of InP in other device areas also. At present, the three other main areas of interest which have evolved for its use are: (a) as a material for solar cell applications, (b) as a semiconductor for FETs, and (c) as a substrate for lattice matched electrooptic devices for fiber optics. Compared to the TED however, these other applications have received little attention worldwide. However, in the United States the primary driving force for InP materials technology development appears to be in the area of lattice matched electrooptic devices.

With any device technology, no matter how fine the arguments for improved device performance nor how good is the actual proven performance of prototype devices, the fact remains that no device is viable until the materials technology is well developed. At present, in the writers' opinion, this cannot be said to have occurred for InP, especially in the United States. Although high quality bulk material has been grown and to a lesser extent epitaxial material, its extremely limited availability makes device investigations very restrictive. As a result, there are no InP devices commercially available today due to the lack of a viable InP materials technology. Conversely, a sufficient InP materials technology will not be developed until additional funds are made available for materials development and the flow of these funds being contingent upon the development of additional markets and needs for microwave and millimeter wave InP devices. Thus not only is a good materials technology necessary to the development of InP devices, but system needs are required to push the materials technology.

2. MATERIALS PREPARATION - BACKGROUND

InP is a compound composed of elements from the 3rd and 5th columns of the periodic table. Like GaAs it is a direct gap semiconductor with an energy gap ~ 1.35 eV and also, like GaAs, it has subsidiary minima in the conduction band accessible to electrons at moderate electric fields. For these reasons InP has the potential for use in a TED and, in fact, a considerable amount of work has been addressed to the fabrication of Gunn devices from this material. Initially, interest was aroused in InP by the proposal that, because of its band structure, more efficient intervalley electron transfer might be observed in this

semiconductor as compared with GaAs. Although the relevance of these early theoretical proposals to current Gunn device operation is somewhat nebulous, the fact remains that TEDs made from InP have attractive characteristics. In particular, it has been found that in addition to higher efficiency, InP Gunn devices have lower noise than those made from GaAs and also are expected to be able to operate to higher frequencies. Compared to Si and GaAs devices, investigations of InP based devices are quite recent. Continued growth of these investigations depends heavily on the demonstration of superior device performance and/or the development of devices where, because of indium phosphide's, intrinsic physical and electrical properties Si and GaAs cannot compete. Theoretically InP has this potential. Some of the vast materials and device technology of Si and GaAs can in many instances be transferred easily to InP and speed its transition from a laboratory curiosity to commercial availability. The first step in this growth cycle is the development of a viable InP materials technology, and the first step in the development of a viable InP materials technology is the development of a readily available source of high quality single crystal material. In the United States, investigations for the preparation of InP for microwave and millimeter wave devices is underway at a limited number of laboratories as shown in Table 1.

Table 1. U. S. Laboratories Investigating InP for Microwave Devices

1.	Bell Telephone Laboratories, Murray Hill, N.J. Bulk and epitaxial growth, molecular beam epitaxy.
2.	Cornell University, Ithaca, NY. Liquid epitaxy.
3.	Crystal Specialties Inc., Monrovia, CA. Bulk growth.
4.	Lincoln Laboratory, Bedford, MA. Bulk growth and liquid epitaxial growth, ion implantation.
5.	Naval Oceanographic Systems Center, San Diego, CA. Liquid and vapor phase epitaxy.
6.	Naval Research Laboratory, Washington, D.C. Bulk and liquid epitaxial growth, ion implantation.
7.	Rome Air Development Center, Bedford, MA. Bulk and vapor phase epitaxial growth and ion implantation.
8.	Stanford Univ., Palo Alto, CA. Electrolytic deposition.
9.	Westinghouse Research Center, Pittsburgh, PA. Vapor phase epitaxy, and ion implantation.
10.	Varian Associates, Palo Alto, CA. Bulk, liquid, and vapor epitaxial growth.

3. BULK SYNTHESIS

The melting point and equilibrium dissociation pressure of InP as determined experimentally by Bachmann and Buehler are respectively 1062°C and 27.5 atm.[3] This high phosphorus pressure at the melting point of InP complicates the growth of bulk single crystals and yet despite this fact, at present, crystal growth from the melt is used exclusively for the growth of bulk InP single crystals. Thus InP single crystals have recently been grown in the United States by the gradient freeze (GF) technique,[4] zone melting,[5] and the liquid encapsulation Czochralski (LEC) method.[6,7,8] Bachmann and his coworkers[9,10] have recently reviewed the current status of InP single crystal growth and have compared the properties of InP crystals grown using the different growth techniques. Their results show that the LEC technique yielded InP single crystals with the best carrier concentration and mobility.

The InP polycrystalline material commercially available in the United States is not sufficiently uniform for single crystal preparation (Tables 2 and 3). Several techniques have been reported for the synthesis of InP.[11-15] However, the highest throughput and greatest purity have been achieved by direct synthesis from the elements. As a result, most laboratories in the United States are currently compounding their polycrystalline InP from the elements prior to liquid encapsulation Czochralski (LEC) growth. The Naval Research Laboratories, MIT Lincoln Laboratory, Varian and Bell Laboratories synthesize InP by a solution growth technique in a horizontal Bridgman or Gradient Freeze system, while direct synthesis at full pressure is being used at Rome Air Development Center (RADC/ET) in heavy walled quartz tubing. All laboratories have vacuum baked the indium at 700°C to 1000°C for approximately 20 hours prior to compounding, to remove volatile impurities – primarily oxygen and zinc. A comparison between the systems used at various laboratories for the preparation of undoped polycrystalline InP is shown in Table 4, and a schematic of a generalized synthesis ampoule and one typical temperature profile used during synthesis are shown in Figure 1.

The source of the phosphorous does not appear critical since individual laboratories have used a number of different sources with no significant differences in results. The limiting factor for the InP compounding appears to be either the indium or the contamination by the reaction vessels. The necessity of prebaking the indium is still open to question since Varian was able to compound poly InP having a mobility of 89,000 with no In prebake; however, the longer growth time (30 days) may effectively act as a prebake by transferring the volatile constituents to the cooler end of the furnace. Further evidence of this or perhaps the presence of two or more different types of electrically active impurities with different segregation coefficients is shown in Table 5[15,16] where for ingot 2, the highest mobility

Table 2. Electrical Properties of Single Crystal Samples Cut From Various Lots of Commercially Available Polycrystalline InP

Supplier Batch No.	T (^{o}K)	ρ (ohm-cm)	n (carriers cm^{-3})	μ ($cm^2 v^{-1} S^{-1}$)	Type
M.C.P. 484	300	0.46	5.0×10^{15}	2600	n
	77	0.08	3.0×10^{15}	25,000	n
M.C.P. 451	300	6.07	1.0×10^{15}	1025	n
	77	60.7	1.6×10^{15}	63	p
M.C.P. 491	300	5.04	1.0×10^{15}	1240	n
	77	10.4	9.3×10^{14}	640	n
M.C.P. 725	300	0.39	4.2×10^{15}	3800	n
	77	0.05	3.7×10^{15}	32,000	n
M.R.L. 1099	300	0.03	1.0×10^{17}	1700	n
	77	0.37	1.0×10^{17}	100	n
M.R.L. 718	300	0.009	3.2×10^{17}	2168	n
	77	0.02	2.9×10^{17}	1027	n
M.R.L. 1102	300	0.003	4.0×10^{18}	490	n
	77	0.002	1.2×10^{19}	260	n
M.R.L. 1554	300	0.11	1.8×10^{16}	3086	n
	77	0.31	1.2×10^{16}	1664	n
M.R.L. 1556	300	0.09	2.1×10^{16}	3800	n
	77	0.14	1.5×10^{16}	5200	n
M.R.L. 1558	300	0.09	2.3×10^{16}	3038	n
	77	0.17	1.6×10^{16}	2351	n

Table 3. Electrical Properties of Single Crystal Samples Cut From Various Lots of Commercially and In-house Compounded Available Polycrystalline InP and Single Crystals Grown From Polycrystalline Material

Undoped Crystals			
Polycrystalline Material and Single Crystal	T (^oK)	n (carriers cm^{-3})	μ ($cm^2 v^{-1} s^{-1}$)
M.R.L. 1099	300	1.0×10^{17}	1700
	77	1.0×10^{17}	100
1-20-H crystal	300	2.7×10^{17}	2300
	77	2.4×10^{17}	2200
M.R.L. 1556	300	2.1×10^{16}	3200
	77	1.5×10^{16}	2900
1-52H crystal	300	7.1×10^{15}	3800
	77	5.7×10^{15}	5200
M.R.L. 1707	300	-	-
	77	-	-
crystal	300	6.4×10^{16}	3000
	77	4.4×10^{16}	4300
M.R.L. 1707	300	-	-
	77	-	-
crystal	300	2.0×10^{16}	2200
	77	1.2×10^{16}	5314
M.C.P. 484	300	5.0×10^{15}	2600
	77	3.0×10^{15}	25,000
1-23-H crystal	300	3.7×10^{15}	3900
	77	2.8×10^{15}	21,000
M.C.P. 726	300	-	-
	77	-	-
crystal	300	4.6×10^{15}	3800
	77	3.8×10^{15}	22,500

Table 3. Electrical Properties of Single Crystal Samples Cut From Various Lots of Commercially and In-house Compounded Available Polycrystalline InP and Single Crystals Grown From Polycrystalline Material (Cont.)

Polycrystalline Material and Single Crystal		T (^oK)	n (carriers cm^{-3})	μ ($cm^2 v^{-1} s^{-1}$)
M.C.P. 702		300	-	-
		77	-	-
crystal		300	5.9×10^{15}	3900
		77	4.9×10^{15}	24,000
M.C.P. 725		300	-	-
		77	-	-
crystal		300	3.9×10^{15}	3900
		77	3.5×10^{15}	24,000
M.C.P. 707		300	-	-
		77	-	-
crystal		300	4.3×10^{15}	4200
		77	3.7×10^{15}	27,900
NRL Syn A		77	2.3×10^{15}	39,800
" " B		77	2.4×10^{15}	45,700
1-83-H crystal		77	2.2×10^{15}	24,800
NRL Syn C		77	2.1×10^{15}	27,600
" " D		77	4.7×10^{15}	26,300
1-81-H crystal		77	4.3×10^{15}	30,324
Doped Crystals				
	ρ (ohm cm)			
M.R.L. 1099 Fe 0.15%	16	77	1.4×10^{15}	300
M.R.L. 1099 Fe 0.15%	0.31	77	3.6×10^{16}	600
M.C.P. 490 Cr 0.13%	3×10^4	77	7.6×10^{10}	2900
M.C.P. 491 Sn $2 \times 10^{16} cm^{-3}$ Cr 0.13%	5×10^3	77	5.4×10^{11}	2900
M.C.P. 490 Fe 0.15%	1.3×10^7	77	1×10^{11}	200
M.C.P. 481 Fe 0.09%	2×10^2	77	7×10^{14}	400

Table 4. Comparison of the Synthesis Conditions and Electrical Properties of Polycrystalline InP Prepared in U. S. Laboratories

Conditions or Electrical Properties	Varian	NRL	RADC/ET	Lincoln
Temperature of Indium - ^{o}C	940	1057	1070-1110	1050-1100
Temperature of Phosphorous - ^{o}C	420	480-500	545	430-490
Growth Pressure - Atm.	2.5	8-15	27.5	4-14
Gradient at Growth - $^{o}C/cm$	15	4.7	None	4
Rate of Growth - cm/hr	0.042	0.17-0.34	None	0.1 cm
Time for Each Run and Product Weight - days/gms	30/500-1500	3/100	3/80	7/500
$77^{o}K$ Carrier Concentration of Best Material Grown to Date - carriers/cm^3	6.8×10^{14}	2.4×10^{15}	-	1×10^{15}
$77^{o}K$ Mobility of Best Material Grown to Date - cm^2/volt-sec	91,000	46,000	-	52,000

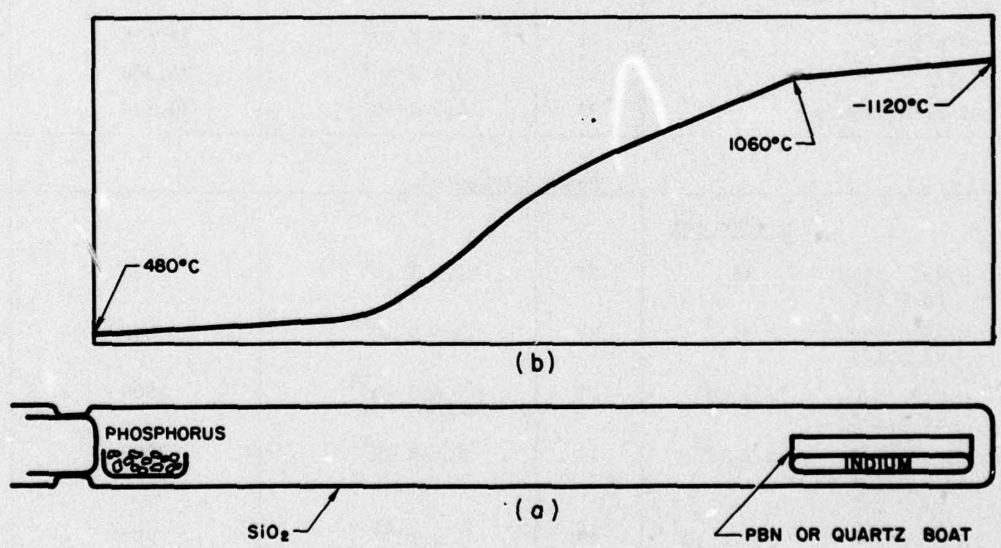

Figure 1. Typical InP Synthesis Apparatus: (a) Schematic of generalized synthesis ampoule, and (b) temperature profile for synthesis at NRL and Lincoln Laboratory

Table 5. Electrical Properties of Varian Polycrystalline InP

Ingot	Section of Ingot	$N_D - N_A$ (cm^{-3}) 300°K	77°K	Mobility (cm^2/volt-sec) 300°K	77°K
1	First to freeze	6.9×10^{14}	6.8×10^{14}	5430	91,000
1	Last to freeze	4.8×10^{15}	3.9×10^{15}	4640	31,780
2	First to freeze	8.5×10^{14}	8.1×10^{14}	5280	76,680
2	Middle section	4.4×10^{14}	4.2×10^{14}	5870	85,960

Ingot	Resistivity (ohm-cm) 300°K	77°K	Indium Preparation
1	1.67	1.14	Vacuum baked at 1000°C for 24 hours
1	0.28	0.05	
2	1.40	0.10	Not baked
2	2.25	0.17	

material was found in the center section of the ingot. NRL uses pyrolytic boron nitride (PBN) crucibles for the indium in the compounding, whereas Varian uses quartz. It is not apparent that silicon containers present the same problems in InP which they do in GaAs. The dominant impurities seen in the InP at compounding are silicon and zinc; nearly all indium has some residual zinc as a shallow acceptor.

4. SINGLE CRYSTAL GROWTH

For both FET and planar TED development, the availability of a high resistivity form of InP for use as a semiinsulating substrate is mandatory. GaAs substrates with resistivities of $\gtrsim 10^8$ ohm-cm obtained by deep level compensation with chromium or oxygen, have been available in limited supplies for a number of years. Attempts to Cr dope InP generally lead to resistivity of $\sim 10^3$ to 10^4 ohm-cm. A compilation is the segregation of Cr at high concentrations giving rise to

a second phase precipitate of CrP by a eutectic reaction identified by Straughan, et al.[17]

Subsequent work has led to approximately one order of magnitude increase in resistivity using Cr.[7] However, the major problem to achieving high resistivity, namely, the solubility limitation and distribution coefficient of Cr in InP, remained. The use of another deep level impurity, viz, Fe, gave much better results. Thus, using Fe as a dopant, Mizuno and Watanabe[18] were able to produce semiinsulating crystals of InP having resistivities in excess of 10^7 ohm-cm. Using iron doping, the solubility is nearly the same as for Cr but the segregation coefficient for Fe is an order of magnitude higher and therefore the resistivity of the resulting crystals can be dramatically increased.[12] The advantages of iron doping are clearly shown in Table 6. Pande and Roberts have shown that both the Cr- and Fe-doped material is nonextrinsic[19] with deep levels at 0.2 eV and 0.5 eV in the case of Cr-doping and 0.2 and 1.12 eV for the Fe-doped material. Such resistivity values are adequate for all presently anticipated or envisioned device applications, provided they can be maintained throughout subsequent fabrication and processing cycles. Iron doping is now used almost exclusively to grow semiinsulating InP crystals, and resistivities of $>10^7$ ohm-cm are routinely achieved (Table 7). In addition, a large number of dopants have been used to grow high quality n and p type crystals over the entire practical range of carrier concentrations.[20, 21]

Table 6. Dopants for Semiinsulating InP*

	M = Fe	M = Cr
[M] in melt	0.3 wt. %	0.3 wt. %
[M] in crystal	$2.5 \times 10^{17}/cm^3$	$2 \times 10^{16}/cm^3$
K_{eff}	1.6×10^{-3}	1.1×10^{-4}
Resistivity	10^7 ohm-cm	10^3-10^5 ohm-cm

*R.L. Henry and E.M. Swiggard, to be published.

Table 7. Fe-doped InP

Crystal	Fe (wt. %)	ρ (ohm-cm)
1-26-H (NRL)	0.15	$>10^7$
1-74-H (NRL)	0.08	$>10^7$
1-85-H (NRL)	0.015	$>10^7$
1-91-H (NRL)	0.015	$>10^7$
1-94-H (NRL)	0.015	$>10^7$
512-77 (RADC)	0.02	$>10^7$

In the United States bulk single crystals of InP are grown almost exclusively by the LEC technique originally described by Mullin, et al.[22] A schematic of the apparatus used for LEC growth is shown in Figure 2. However, upgrading of the LEC apparatus to include the more sophisticated automatic diameter control described by Bardsley[23] has not yet been accomplished. There are minor variations between the growth techniques used at the various laboratories. For example, the speed and/or direction of rotation of both the seed and crucible, the rate of growth, the nature of the crucible (quartz or pyrolytic boron nitride, PBN), and the use of an "as purchased" B_2O_3 pellet or a predried B_2O_3 pellet which has undergone an 1000°C+ baking cycle immediately prior to use. Regardless of these differences, however, all have been able to grow undoped InP crystals having similar properties. These growth efforts are small and the availability of InP substrates in the United States is very limited. The main source is Metals Research in England, while small experimental quantities are available from Varian, NRL, and RADC/ET. In addition to the efforts to grow single crystal InP by the LEC technique, Crystal Specialties, Inc., a commercial supplier of high quality GaAs single crystals grown by a combination gradient freeze - Bridgman technique, is currently investigating the growth of InP using a high pressure gradient freeze apparatus under an RADC/ET contract. In this effort Crystal Specialties, Inc., expects to benefit greatly by a technology transfer of their already developed expertise in GaAs.

The three major problems encountered in the growth of device quality bulk single crystals of InP are: (a) the reduction of unintentionally introduced impurity levels, (b) the elimination of twinning and, (c) the reduction of dislocation densities. As already discussed, the problem of the reduction of impurity levels is

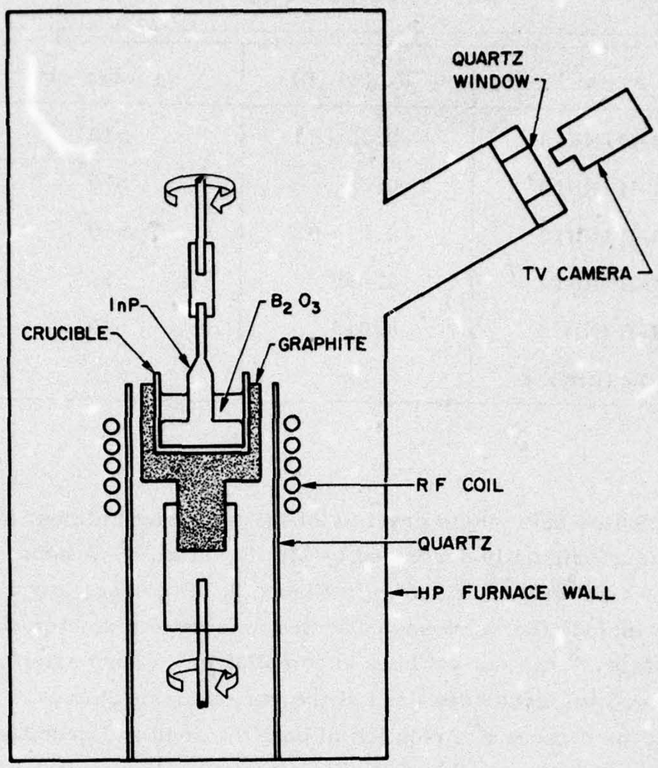

Figure 2. Schematic of LEC Growth Chamber

being attacked by careful preparation of the polycrystalline feed material. However, it is interesting to note that even if high purity, high mobility material is used as the starting material, the crystals generally have properties similar to those grown from lower mobility starting material. Most likely the boron oxide encapsulant is giving a residual impurity level which is independent of the starting compound purity. In addition, although NRL has shown the advantage of PBN for the preparation and growth of GaAs,[8] it appears that the pyrolytic boron nitride ware does not result in significantly purer InP than the use of silica boats and crucibles.[4,12] Nevertheless undoped InP crystals being grown in the United States are of high quality with average carrier concentrations below 5×10^{15} carriers/cm^3 and average liquid nitrogen mobilities between 25,000 and 30,000 cm^2/volt-sec. Twinning is a serious problem that greatly reduces the efficiency and cost effectiveness of LEC growth. Lack of stoichiometry, seed orientation and pronounced edge faceting[24] as well as foreign particles and gas bubbles trapped in the B_2O_3 encapsulant[22] all contribute to the twinning problem. Careful attention to

the control and elimination of these sources of trouble has greatly reduced the incident of twinning thereby increasing crystal yield. However, no overall growth procedure has been found which completely eliminates the twinning problem. The growth of InP crystals having low dislocation densities appears to be under excellent control. Borrowing heavily from the technology evolved for the growth of low dislocation GaAs,[25] InP crystals with dislocation densities comparable to available good GaAs crystals have been grown. In fact, Seki, et al.[20] have been able to achieve zero dislocation InP 5-10 mm from the seed in undoped, and n and p type crystals when the standard necking in procedure was used. One rather surprising finding in this paper was that in heavily doped (Zn and S in the $3\text{-}5 \times 10^{18}$ carriers/cm^3 range) crystals, the entire crystal had zero dislocations. However, in the undoped cases, dislocations increased when the crystal shoulder was formed. Seki, et al.[20] attribute this phenomena to the fact that both S and Zn form high energy bonds in InP which pin dislocations introduced at the periphery of the crystal by thermal stress. Antypas[26] recently reported on the dislocation density at the top of two crystals grown from his high purity stoichiometric polycrystalline material.[15] The first, a Cr doped crystal, had an almost uniform $10^3/cm^2$ dislocation while the Sn (5×10^{17}) doped crystal, which was approximately 17.5 mm in diameter, had an EPD of 10^4 at the edges but was zero dislocation over the entire middle section. In general, however, the dislocation densities of InP single crystals grown at most laboratories in the United States have nominal values between 10^3 to 10^4 cm^{-2}.

As mentioned above, all of the single crystal InP currently being grown in the United States is grown by the LEC technique. Crystal Specialties, Inc., however, is currently setting up equipment to grow single crystal InP by a modified Bridgman - Gradient Freeze technique. This technique has been successfully used by Crystal Specialties for several years for the commercial production of GaAs for microwave and electrooptic applications. The main problem involved in the successful transfer of the technology developed for GaAs to the growth of high purity InP is the high pressure developed by InP at its melting point. To cope with this problem Crystal Specialties, Inc., has designed and built a high pressure vessel in which the synthesis and growth will be carried out. During synthesis and growth a sensor attached to ampoule will be used to dynamically balance the pressures inside the ampoule and its containing high pressure vessel. Figure 3 is a cross sectional view of the growth apparatus. Because of its lower melting point and the fact that InP does not wet quartz, the growth of InP is expected to be easier than the growth of GaAs.

Compared to growth by the Liquid Encapsulation technique this system has several advantages for the growth of InP. It is inherently simpler and far less costly. Synthesis and growth are a one-step process which is expected to be

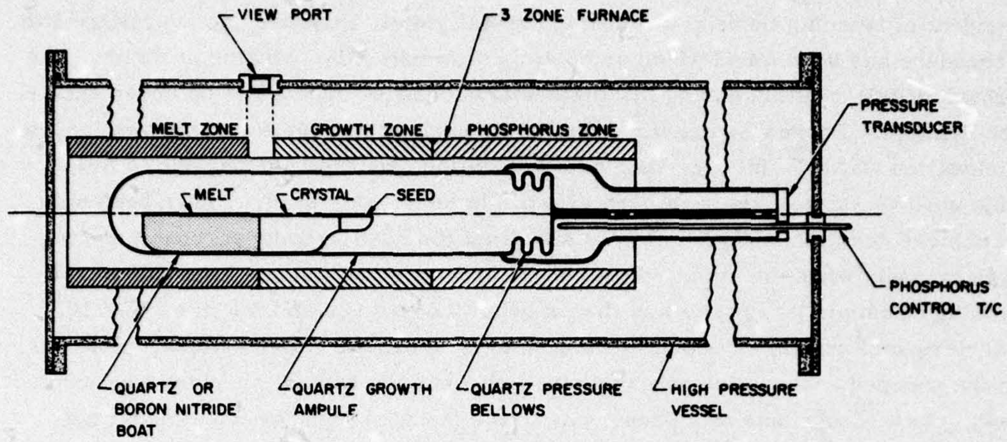

Figure 3. High Pressure InP Growth System

accomplished in 18 hours. The twinning problem should be greatly reduced since the stoichiometry of the melt can be easily controlled and bubbles and foreign particles at the growth interface are eliminated. If successful, therefore, the technique should provide a low cost alternative for the growth of high quality single crystal InP.

It is known in the case of GaAs that both heat treatment of the substrate prior to layer growth, as well as any subsequent annealing of the film can lead to degrading effects at the surfaces. A similar effect, although apparently less in Fe-doped than in Cr-doped material, occurs in a pronounced fashion in InP presumably as a result of the high vapor pressure of P.[27,28] Williams and McGovern[29] have reported on the observation of phosphorus diffusion from vapor phase epitaxy (VPE) InP during annealing at temperatures in excess of 320°C and it may presumably be expected that such effects will also occur in bulk material. Farrow[30] has demonstrated a reduction in thermal degradation of the (100) surfaces of bulk InP by use of an impinging molecular beam of P. This technique, although of use in certain applications, would seem to be of limited applicability in the case of epilayer growth. The somewhat analogous process of using a P overpressure is, however, used with success in the growth of epitaxial films. It, at present, has become an almost universal practice to circumvent the substrate degradation[31] which invariably occurs at the temperatures employed for layer growth by preceding the growth cycle by either a chemical vapor-etch in the case of VPE or an In-etch,[32] or a "meltback" in the case of liquid phase epitaxy (LPE). Subsequent processing, during such cycles as contact alloying and high temperature dielectric deposition, should always be conducted with an awareness of the possible consequences to the

electrical and crystallographic properties of the exposed sample surfaces.[33] Thus, in ion implantation where the implanted substrate must be annealed at temperatures of 600°C to 800°C, Davies has found that surface integrity can be maintained by the use of either a Si_3N_4 cap or heat treating the sample in a PH_3 atmosphere.[34]

5. EPITAXY

The first report of epitaxial growth of InP appeared in 1969.[35] This material, grown by vapor phase transport on <100>-oriented InAs substrates, had net electron densities in the range of 5×10^{15} to 1×10^{16} cm^{-3} and mobilities as high as 18,000 cm^2/V-sec. at 77K. Although others have reported on heteroepitaxial growth,[36, 37] subsequent work, as a result of the increasing if albeit limited availability of good quality substrate material, has concentrated mainly on homoepitaxy. Liquid phase growth using both tipping[38, 39] and sliding boat[40, 43] procedures as well as vapor phase growth[44-52] have all been used. As with GaAs there are advantages and disadvantages with both methods. Primarily, liquid phase growth has the advantage of simplicity, low cost, and the potential, using a sliding boat, of straightforwardly being applied to the growth of multilayer structures for, for example, laser diode and TED and FET applications.

The purest LPE InP reported in the United States is that of the Cornell University group where a mobility of 67,000 cm^2/V-sec and an uncompensated electron concentration of $1.2 \times 10^{15}/cm^3$ at 77K were achieved.[41] The work is based on the assumption that volatile components (most likely Si and Zn) are present in the indium and a long bake out time will result in In purification as shown in Figure 4, where the Si concentration apparently decreased with increasing baking time. They project that part of the Si comes from the dissociation of SiO_2 by water vapor in the hot furnace tube. The LPE process appears to consistently yield higher mobility and lower defect density InP if the wipe off or etch bach technique is used similar to the results[32] obtained for GaAs.[42] Vapor Phase Epitaxy (VPE) is inherently a higher cost, more complicated method of epitaxy than LPE. However, because of the availability of higher purity source and system materials and the applicability of the mole fraction effect, first noted in GaAs, the highest purity InP layers produced to date have been grown by VPE both in England and the United States. Thus, both Clarke[46] and Fairman, et al[48] have reported the growth of high purity InP epitaxial layers with carrier concentrations in the mid- to low-$10^{13}/cm^3$ range and liquid nitrogen mobilities in excess of $10^4 cm^2$/volt-sec. in a $PCl_3/In/H_2$ system such as that shown schematically in Figure 5. VPE also, in practice, seems to result in smoother and more uniform layer growth. Growth

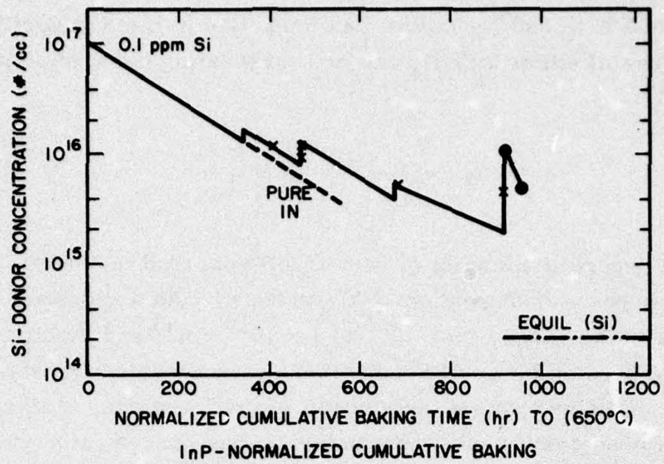

Figure 4. Silicon Concentration vs Baking Time (V. Wrick et al, 19th Electronic Materials Conf., Ithaca, N. Y., 1977)

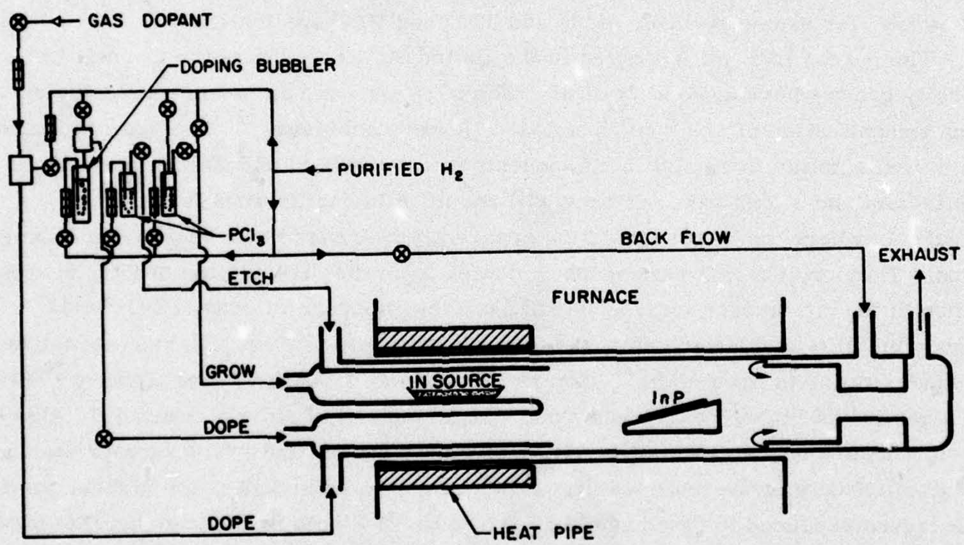

Figure 5. Vapor Phase Epitaxial System for InP (Courtesy of V. Wrick)

from the vapor phase also lends itself more easily to the control of doping profiles[48, 52] because of the inherent analog nature of the technique.

Considering the growth difficulty and the disagreement that exists over the benefits of buffer layers on GaAs, the lack of published information on buffer layer growth in InP is not surprising. It is known, however, that work is underway on the growth of buffer layers on this material at a number of laboratories including Plessey where 10^6 Ω - cm material has been produced.

As with any material the growth of single crystal InP is an exceedingly complex process. At present, more effort would seem to be being applied to the vapor phase process but in neither case is the method well understood.

Perhaps in part because of this, a number of alternative techniques for the preparation of layers of this semiconductor have been tried. Eastman at Cornell University has applied Peltier cooling to nucleate layers of InP from the melt This method supposedly enables faster and more uniform growth rates to be obtained than is possible using the more usually employed temperature lowering methods resulting in improvements in control and impurity levels. Thermal evaporation of InP using both Knudsen and Langmuir conditions has been reported by Farrow.[53] Fraas, et al[54] have grown heteroepitaxial layers on GaAs and CdS substrates using planar reactive deposition and workers, primarily at Bell Laboratories, have grown InP using molecular beam epitaxy.[55, 56, 57] Ion-implantation of impurities into semiinsulating substrate material[58] is also a technique which offers promise for an alternative to the more conventional LPE and VPE growth for the preparation of thin conducting layers. All of these alternate methods offer the potential, which in part has already been demonstrated, for the fast preparation of large areas of very uniform material. Such uniformity, both in thickness and carrier density, is paramount for the reproducible high yield production of devices from this semiconductor as is also the necessity of a good surface finish on the epitaxial layers.[40, 55, 59]

6. MATERIALS CHARACTERIZATION

Despite the fact that the attention of the device physicist has only relatively recently been attracted to InP, this semiconductor has received considerable attention from the point-of-view of its fundamental physical and electrical characteristics. A tabulation of the principal parameters of this semiconductor, as they are presently understood, appears in Table 8.

The electrical properties of resistivity and Hall coefficient are perhaps the most widely-studied characteristics of this material. The results of the earliest measurements have been summarized elsewhere.[1] Since then, Blood and Orton[60]

Table 8. Summary of Selected Experimental and Theoretical (in parentheses) Properties of InP and GaAs

	InP	GaAs
Density	4.79	5.37 (g/cm^3)
Effective mass		
(000) valley	0.08	0.067
(100)		0.35
(111)	0.04	
Intervalley separation	0.06	0.36 (eV)
Static ε	12.35	12.53
Optical ε	9.52	10.82
Deformation potential	7.0 ((000) valley) 12.0 ((111) valley)	7.0
Velocity of sound	5.3 x 10^5	5.22 x 10^5 cm/sec
Threshold field	10.0 (10.0)	3.5 (3.5) kV/cm
Peak velocity	2.4 (2.4)	1.9 (2.1) cm/sec
Saturation velocity	0.5	0.95 (0.75→0.85)
Breakdown field	1.4 (1.3)	0.87 (0.8→1.0) kV/cm
Peak to valley Ratio	4.8 (4.1)	2.0 (2.3)
Energy relaxation time ((000) valley)	2 x 10^{-12} at low E 3 x 10^{-12} near threshold	6 x 10^{-12}
Thermal Conductivity	0.7	0.54 W/cm ^{o}K
Mobility (highest purity)		
electron	4,500 at 300K >140,000 at 77K	8,200 cm^2/V-sec at 300K 200,000 " " at 77K
hole	150 at 300K 1,200 at 77K	3,000 " " at 300K 4,000 " " at 77K
Lifetime at 300K		
electron	∿ 1 msec	∿ 1 μsec
hole	∿ 1 μsec	∿ 2 nsec

The above values are meant only to be representative of the available data. For numerical work the original references should be consulted.

have considerably extended the range of these measurements by characterizing the resistivity and Hall coefficient of n-type VPE InP over the wide temperature range 5 to 400K and the magnetoresistance mobility of LPE material from 300 to 700K. The lower temperature measurements indicated that the mobility exhibited a typical peak value of 25,000 cm^2/V-sec. near 70K with ionized impurity scattering being dominant at lower temperatures and polar phonons dominating above the peak. At low temperatures (<15K) an increased value of apparent carrier concentration was observed in almost all the samples which was interpreted as being due to impurity conduction. This conduction mechanism, involving a phonon-activated hopping of electrons between donor sites, empty by virtue of the presence of a compensating species, has also been reported by Emel'yanenko, et al.[61] The higher temperature measurements showed that the mobility continues to decrease with increasing temperature in good agreement with earlier theories,[62] with no apparent reduction due to electron transfer to higher conduction band minima as is observed in GaAs. This result is, of course, quite consistent with the higher Γ - X separation in this semiconductor.

High field transport effects in InP have been reported by Herbert, et al[63] where they consider in some detail the calculation of the velocity-field curve for this semiconductor. Primarily this paper presents revised estimates for the low-energy LA phonons which more closely agree with the experimental values. Topics such as the contribution of alloy scattering and carrier screening are included. The related topic of the avalanche multiplication of carriers has been considered by Molodyan, et al[64] using p-n junctions fabricated by the diffusion of zinc into n-type InP plates of carrier density ~ 0.9 to 5.0×10^{16} cm^{-3}. Filtered illumination was used to measure the dependence of photocurrent on reverse bias. Their data suggested a mean-free path of between 120 Å and 170 Å for hot electrons scattered by optical phonons (energy = 0.043 eV), a value of 1.7 ± 0.1 eV being obtained for the threshold for avalanche.

This same paper also reported values of 2.5 to 3.0 μm and 10^{-8} sec for the sum of the electron and hole diffusion lengths and lifetime of carriers respectively in the InP. Chang and Meijer[65] have also reported on the determination of diffusion length using an entirely different technique. These workers measured photoemissive yield as a function of incident photon energy for p-type samples of carrier concentration $\sim 5 \times 10^{18}$ cm^{-3} from which they deduced a value for the diffusion length of electrons of 0.53 μm, a value somewhat lower than that reported by Molodyan, et al.[64] This is perhaps not inconsistent when the differences in the samples employed (doping level, etc.) are taken into consideration. The effects of pressure on the band structure and hence on the high field threshold for transferred electron effects has been reported by Pitt and Vyas.[66] These authors discuss the current understanding that exists on the location of the band extrema in InP as well

as the problems confronting the "three level model." They show that the lowest (Γ) minimum in InP moves upward in energy away from the valence band at a rate of 9.5×10^{-6} eV bar^{-1}, while the next highest (L) minimum rises at a slower rate of 2 to 3×10^{-6} eV bar^{-1}. In contrast with these two extrema, the initially higher X minimum drops toward the valence band at -2×10^{-6} eV bar so that at a pressure ~70 kbar the three extrema coincide. Variations in samples due to differences in contact properties were identified. Despite this, it seems as though there is little variation in the threshold field for oscillation to pressures as high as 40 kbar presumably due to changes in the high field polar optical mode scattering which dominates in these samples. Above 40 kbar the threshold for oscillation increases until at ~55 kbar oscillations cease.

Band structure parameters, which apart from transport studies occupy perhaps the largest single body of data on this semiconductor have been studied by a number of techniques, many of them optical. Ley, et al[67] have reported on photoemission studies on a number of III-V and II-VI compounds from which they determined values for the binding energies of the outermost d-shells as well as the location of the Fermi level at the surface. For reasons not obvious to the authors, InP was omitted from this latter tabulation.

The determination of a light and heavy hole effective mass value of 0.2 ± 0.01 and 0.06 ± 0.02 respectively, in the <111> direction was reported by Leatin, et al.[68] These authors used cyclotron resonance in p-type samples generated by carriers excited from impurity states at 110K by the 337 μm radiation from a HCN laser together with pulsed magnetic fields as high as 350 kG to determine these valence band parameters. In addition, their results enabled an estimate of the Dresselhaus parameters to be made viz. $A = -5.04$, $|B| = 3.12$ and $C^2 = 6.57$.

A subject which has received a considerable amount of experimental attention is that of excitonic effects in this material. Losch and Fischbach[69] made high resolution absorption measurements between 1.4 and 1.64 eV on InP by measuring the photoluminescence emanating from Schottky diodes at 1.8K. By altering the bias and hence the extent of the depletion layer, the intensity of the emitted radiation could be modulated from which it is possible to calculate the absorption of the incident radiation. Spectra taken in such a fashion indicated a very sharp exciton absorption line at 1.4183 eV together with a line and a shoulder at lower energies due to bound excitons. Additional electroreflectance measurements allowed for the determination of the spin orbit splitting of the valence band in these samples of 99 ± 4 meV. Nam, et al[70] also reported on photoluminescence measurements made on unintentionally doped InP epilayers using the 6471Å radiation from a krypton-ion laser. These authors observed for the first time the spectra for the excited states of the free exciton in InP from which a value of $(4.8 \pm 0.2) \times 10^{-3}$ eV was deduced for the exciton binding energy. Values for the bandgap, the electron

Zeeman splitting factor and the hole splitting parameter were also determined as 1.4233 ± 0.0002 eV, 1.2 ± 0.2, and 0.86 ± 0.08 respectively. Reynolds et al[71] also reported on photoluminescence measurements made with the same experimental setup. These authors were primarily concerned with the optical transitions associated with the decay of bound-exciton-donor complexes. Their spectra showed a large amount of detail which, by comparison with theory, enabled them to deduce a value of 7.38 ± 0.01 meV for the donor binding energy (the chemical nature of the donors being unknown). Combining this with an electron effective mass value of 0.081 gave a value for the static dielectric contact for InP of 12.21 ± 0.05, a value in good agreement with existing data.[72, 73]

Reflectance spectra in the region just below the bandgap energy, like photoluminescence, will also discern exciton effects. Such measurements have been reported by Evangelisti, et al.[74] These authors made measurements at 2K on both bulk and epitaxial material both on the "free surface" as well as on Schottky diodes prepared with semitransparent Au electrodes. With the latter the reflected light is a function both of interference effects and absorption of the light in the space charge region. Both of these effects are a function of bias through both the dependence of the physical extent of the depletion layer as well as through the contribution of field dependent absorption (Franz-Keldysh effect). Analysis of their spectra enabled these authors to deduce a value of 1.4185 eV for the transverse exciton energy and 4.9 meV for the effective Rydberg energy. Reflectance was also measured as a function of magnetic field by Willmann, et al.[75] From their results these authors deduced values for both the electron and hole g values as well as the Luttinger band parameters.

Popov[76] has studied the effect of residual Si and C impurities on the photoluminescence properties of bulk InP crystals and Göbel, et al[77] have examined how the doping concentration affects the shift in the luminescence peaks with intensity. Using tellurium doped bulk samples they observed that for electron densities below 10^{18} cm^{-3} the photoluminescence maximum shifted to lower energies with increasing excitation intensity. Above this carrier concentration the shift was observed to higher energies. They conclude that below a critical concentration $\gtrsim 10^{17}$ cm^{-3} the main effect contributing to the observed shift is an exciton-exciton interaction, whereas above this critical concentration excitons are absent because of electron screening and the main contribution is due to the filling of the conduction band states (Burstein-Moss effect). Backmann, et al[9] have made $77^{o}K$ photoluminescence measurements on p-type LEC grown crystals and have identified peaks due to Zn, Mg, Be and Mn.

Spicer, et al[78] have examined core level shifts resulting from oxygen adsorption in submonolayer quantities by photoemission measurements using synchrotron radiation. They find that oxidation of GaAs and InP resulted in the preferential

removal of electrons from the column V element leaving the column III element unaffected, whereas for GaSb both constituents were involved. Phonon line shape dependence on surface preparation has been studied via surface reflection Raman scattering by Evans and Ushiode.[79] They observed variations with polishing and annealing which they ascribed to the effects of strain and crystal damage. Two phonon processes and their contribution to the far infrared absorption in InP have been reported by Koteles and Dators.[80]

Rochon and Fortin[81] have measured the spectral distribution of the photovoltage generated by Au/InP Schottky barriers in magnetic fields of up to 70 kG and have observed an oscillatory response which, when corrected for exciton binding effects, gave values for a number of band parameters. Specifically, they obtain for the conduction band effective mass a value of 0.079 ± 0.001, from the split-off valence to conduction band transition a spin-orbit splitting energy of 0.108 ± 0.003 eV with a split-off hole effective mass of $\sim 0.21 \pm 0.02$, these values being in good agreement with those reported elsewhere.[69] Luttinger parameter values were also estimated.

From an analysis of the spectral oscillations observed in the photoelectromagnetic effect in a quantizing magnetic field at 4.2K, Barbarie and Fortin[82] have also deduced a value for the spin-orbit splitting of the valence band of 0.102 ± 0.006 eV. They also reported a LO phonon energy of 36 meV.

Finally we might note that Kovalevskaya, et al[83] have observed a shift in the spectral sensitivity of InP p-i-ν diode optical detectors with reverse bias. They interpret their data as being quite consistent with the Franz-Keldysh dependence of absorption on electric field. Weisbuch and Hermann[84] studied the polarization of the photoluminescence of InP samples immersed in an oscillating magnetic field as a function of a superimposed dc magnetic field. Such a conduction electron spin resonance experiment led to a polarization peak at 1.7K at a magnetic field of $\sim$80G from which they deduced a value for the g factor of 1.26 ± 0.05. Boyle and Sladek[85] have examined ultrasonic wave propagation in InP at 30, 90, and 150 MHz in the <111> direction. From their results they conclude that the piezoelectric constant for InP has a value of 0.040 ± 0.002 C/m^2, a value smaller than that of any other III-V material so far investigated and in total disagreement with the value of 0.29 C/m^2 predicted[86] on the basis of a rigid ion model for this semiconductor.

7. InP DEVICES - THE MOTIVATION

The characteristics of solid-state devices are limited fundamentally to a performance determined by the properties of the semiconductor from which they are made. Parasitics resulting from the design and fabrication procedures employed, temper the results, but in the final analysis it is the transport and band structure characteristics of the material which are the determining factors. It is for such reasons that InP is of interest. There are other materials with even more attractive properties than InP, but in all such cases very little is usually known about their growth.

It was the proposal, made in 1970[2] that because of its band structure higher efficiency transferred electron effects might be seen in InP, that initiated interest in this semiconductor. The argument, which has been reviewed in detail elsewhere,[1] consisted basically in the reasoning that because the coupling between the lowest (Γ) minimum and the upper (X) minima is stronger than that between the Γ and the lowest (L) subsidiary minima, the intervalley transfer in a high electric field will occur $\Gamma \rightarrow X \rightarrow L$ rather than $\Gamma \rightarrow L$ as is the case in GaAs. The result of such a "three-level" effect was predicted to be an increased peak-to-valley ratio and a steeper transition in the negative resistance range, both effects being expected to lead to an enhanced dc to microwave conversion efficiency in a TED. The subsequent refutation of this model,[87] however, in no way detracts from the attractiveness of InP.

7.1 Carrier Velocity

Because of the central importance of carrier mobility in determining the operation of microwave devices, a considerable body of literature, both experimental and theoretical, has grown up around the subject of the static velocity field characteristics of InP. Figure 6 shows curves for InP, GaAs, and Si which are representative of not only the available data but also the theoretical calculations which exist at present for these materials. It is evident that in contrast with Si, InP like GaAs possesses a region of negative differential mobility which is used to advantage in the TED. It can also be seen that, whereas the low field mobility of InP (4000 cm^2/V-sec.) is somewhat less than that of GaAs (8600 cm^2/V-sec.) because of the increased separation between the primary and lowest subsidiary conduction band minima, the velocity of carriers in InP rises above the maximum attainable in GaAs to a value near 3×10^7 cm/sec at an electric field threshold for intervalley transfer at ~ 10 kV/cm.

A large number of theoretical calculations as well as a wide variety of experimental determinations of the v/E characteristics of InP have been made.[87, 88] Although the spread in experimental results has been wide, a general concensus

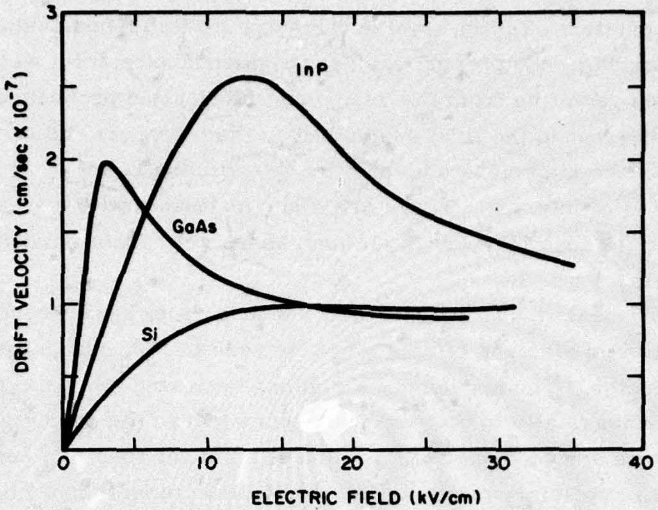

Figure 6. Drift Velocity vs Electric Field for GaAs, Si, and InP

has tended to emerge which is in reasonably good agreement with the most generally accepted theoretical procedure based on a Monte Carlo computer simulation of the electron dynamics involved. From this body of knowledge we may state with reasonable confidence the following for InP (GaAs values in parenthesis): A threshold field ~10 kV/cm (3.5 kV/cm), a peak velocity $\sim 2.4 \times 10^7$ cm/sec. (2.0×10^7 cm/sec.), a saturation velocity $\sim 0.5 \times 10^7$ cm/sec. (0.9×10^7 cm/sec.), and a peak-to-valley ratio of ~4.5 compared to ~2.0 for GaAs. Ridley[88] has also calculated that despite the smaller bandgap in InP compared with GaAs, the high field threshold for avalanche breakdown is higher, viz., 1.4×10^5 V/cm for InP compared to 0.87×10^5 V/cm for GaAs due to the smaller value of the LA-phonon energy in InP resulting from the heavy mass of the In atom. These values are all for 300K conditions. Tebbenham and Walsh[89] and Majerfeld, et al[90] have reported on the effects of temperature on threshold field and peak velocity in epitaxial layers. They found, in agreement with the results of Monte Carlo calculations,[91] that cooling caused a monotonic increase in the peak velocity with values of $\sim 3.3 \times 10^7$ cm/sec at 118 K and 1.9×10^7 cm/sec at 446K being observed. Simultaneously, the threshold field increased from 8 kV/cm to 12.3 kV/cm on heating the sample from 118K to 380K but decreased at higher temperatures. It was also observed that decreasing the thickness of the epilayer from 18.5 to 5 μm led to an increase of the threshold field from 10.0 to 15.1 kV/cm, a fact consistent with the observation in GaAs of the invariable reluctance of very thin epitaxial layers such as are

used in FETs to exhibit oscillatory Gunn phenomena presumably due to the tight "dielectric loading" of the adjacent medium.

Despite the fact that the "3-level" effect originally proposed for InP is no longer considered relevant, a consideration of the previously-stated properties, in particular the large peak-to-valley ratio, leads to the conclusion that InP has advantages over GaAs for TED applications.[88] In addition, the higher avalanche field in InP indicates that FETs made from this material will be capable of yielding higher output powers. In contrast with this, although the carrier velocity at intermediate fields (that is, 3 kV/cm $\lesssim$ E $\lesssim$ 30 kV/cm) is higher in InP than in GaAs, at low and at high fields it is less, which has led Kroemer[92] to conclude that InP would be inferior to GaAs in FET applications. Despite this, many arguments to the contrary have been raised. We shall return to this question later; however, it is worth noting that at present it is still not fully obvious exactly which value of carrier velocity, taken from a curve such as shown in Figure 6, should be used in an estimate of FET performance and, moreover, whether steady state values are relevant at all in the extremely short gate geometries ($\lesssim 1\ \mu$m) that are used in microwave FET structures.[94]

7.2 High Frequency Considerations

The detailed processes which determine the fundamental limits on speed of response of a device can be exceedingly complex. Neglecting parasitic effects it *might be expected, for example,* that in a TED the ultimate response time would be determined by the speed at which an electron might undergo intervalley transfer. It was recognition of the fact that intervalley scattering is faster in InP than in GaAs that led people to initially suspect the advantage of InP over GaAs as a "high speed material." However, as was realized by Rees,[93] with sufficiently fast intervalley scattering, the rate limiting mechanism becomes the rapidity with which carriers may be heated and cooled within the central valley. Even with this perturbation, however, the result remains unchanged; InP should perform better than GaAs at high frequencies. Kroemer[92] has concluded that InP should, in fact, have an ultimate frequency limit about twice that of GaAs and Ridley[88] has calculated the cutoff frequency of InP to be 110 GHz compared to 50 GHz in GaAs.

The other microwave device of interest, namely the FET, does not rely upon intervalley transitions for its operation. In fact such transferred electron effects are eminently undesirable in general in such a device, and by careful device and circuit design can be readily suppressed in all but the highest power devices.

To first order a conceptual understanding of the high frequency limits on a FET is quite straightforward: an electron exiting the source electrode comes under the influence of the space charge due to the gate field on its journey to the drain. If the input to the gate is changing slowly with respect to the time of flight

of the carrier along the channel, then the electron arriving at the drain will faithfully reflect the instantaneous value of the input signal. However, if for example, the gate field should undergo one complete cycle during the time it takes the electron to go from the source to the drain, then the electron at the output will be simply related by a 360° phase shift with respect to its value at the source and hence will appear as unchanged by the gate field.

This simple model, which is supported by experiment, thus indicates that the frequency response in the limit of negligible parasitic loading is determined by the time of flight of carriers between the source and the drain. Specifically, the frequency at which the current gain is unity, f_T, can be calculated from $f_T = v_{EFF}/2\pi L_g$ where L_g is the effective gate length (somewhere between the gate length and the source drain spacing) and v_{EFF} is L_g/τ where τ is the transit time of carriers in the channel. Thus high mobility and short channel length are consistent with good high frequency performance. The latter is a matter of device geometry and is dependent on the semiconductor used only to the extent that the material is amenable to the refined photolithography required for the submicron resolutions employed in state-of-the-art devices. To this extent, InP and GaAs are equivalent. The former, viz., the effect of carrier velocity, is the determining factor in the frequency response of this device. Inspection of Figure 6, however, indicated why even this simple model is not unambiguous in predicting the relative merits of InP and GaAs in this application. As can be seen from this figure at low fields, because of its lower low field mobility, the velocity of carriers is less in InP than in GaAs. Beyond the threshold for electron transfer in GaAs, however, the velocity advantage swings to InP and remains there until the highest fields are reached at which point GaAs once again becomes superior. If the FET were a one-dimensional device the solution would involve simply choosing the operating field and from the velocity/field curve determining the velocity appropriate to each material. However, the FET is in the simplest approximation a two-dimensional device which results in a nonuniform field distribution along the channel. As a result no simple statement can be made as to what the appropriate velocity values are to compare. Intuitively, it is generally concluded that the appropriate velocity is "some average" of the v/E curve over a certain region! From such a statement and the knowledge that much of the channel of the shorter gate length devices are in the high field velocity saturation range, it is not difficult to conclude from such curves as those shown in Figure 6 that InP may indeed be better than GaAs for high frequency FET application. A further complication, however, involves the fact that curves such as those shown in Figure 6 are static curves measured on, or calculated for, bulk samples. Such v/E curves predict domain formation with consequent oscillation for fields above threshold. However, FET devices are rarely observed to exhibit oscillation presumably due to field distortion due to the close proximity of the two

large faces of the active layer which tend to inhibit the formation of the field concentrations associated with a domain. It is thus generally agreed that the static v/E curve is not directly applicable to the situation that prevails in a FET. At present the concensus seems to favor a v/E relationship as shown in Figure 7, that is, a linear low-field region appropriate to the low-field mobility of the material and a saturated constant-velocity region above the field at which carrier transfer would have occurred in the static case. If such a piecewise linear approximation represents the true state in the FET, then it may be concluded that InP does indeed offer speed advantages over GaAs in FET applications.

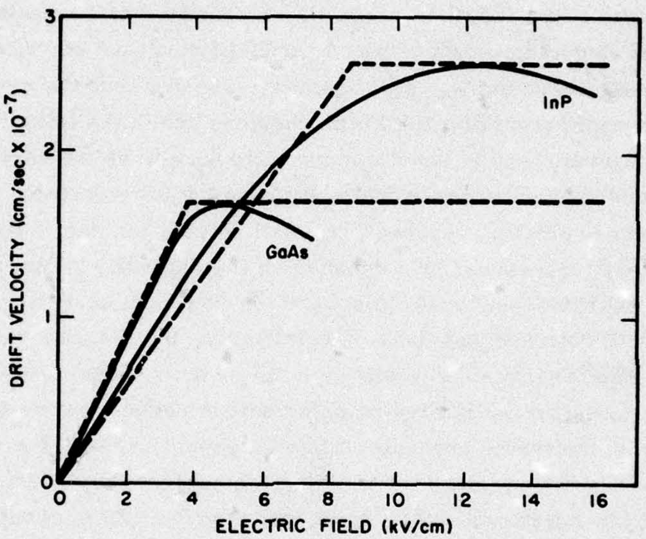

Figure 7. Drift Velocity vs Electric Field for GaAs and InP

Because of the great complexity of device modeling at the detailed level, the above first order arguments can only be considered as a rough approximation at best. Numerical solution, although far more involved, does in general lead to more definitive conclusions. In particular, Monte Carlo calculations rely on fewest questionable assumptions. Such calculations have been undertaken by a number of workers, in particular, Maloney and Frey at Cornell have published extensively on their results of such computations.[94, a, b, 95, 96] Earlier, Monte Carlo calculations by Ruch[97] on Si and GaAs FETs had shown that although the electron velocity in GaAs is greater than that in Si, a further improvement can

result from the velocity overshoot that accompanies the initial stages of the electron's flight. When an electric field is applied to a conductor, the carriers will absorb energy from the field and accelerate in the direction of the field. This will continue until a collision occurs with either an impurity, a defect, or a lattice atom. This transfer of energy to phonon modes will eventually balance the input of energy from the field and a steady state will be set up. At this point a v/E curve such as is shown in either Figures 6 or 7, will represent the electron motion. However, prior to the establishment of the steady state, the carriers may travel with a velocity in excess of their final velocity. The magnitude of this "velocity overshoot," its duration, and the distance travelled by the carriers during this time is a function of the momentum and energy relaxation times in the material and depends on the nature and strength of the associated scattering processes. In semiconductors, because all collisions randomize momentum but only a small amount of energy is carried away by each phonon (for example, ~ 0.05 eV), the momentum relaxation time τ_m is, in general, shorter than the energy relaxation time τ_E. On application of a field, the carriers reach the lattice temperature in a time τ_m. However, this is short compared to τ_E and so the carriers will continue to gain energy and increase their temperature for a further time ($\tau_E - \tau_m$). During this period of velocity overshoot, τ_m will be reduced due to its energy dependence. Velocity overshoot thus depends on the disparity between τ_E and τ_m as well as on its energy dependence. Because the dominant scattering process in the central valley of both InP and GaAs is polar optic, the frequency of which is almost independent of energy, there will be little or no overshoot. However, fields sufficiently large to cause intervalley transfer will introduce the necessary energy dependence into the scattering process. Thus we expect to see the effect of the transient dynamics of the carriers manifesting themselves only in the shorter gate devices at all but the lowest voltages. In Si, the steady state is always reached in less than 1 picosecond during which time the carriers travel less than $0.1\ \mu m$. Such an effect is thus negligible in practical devices. In direct gap materials such as GaAs and InP, however, this is not the case. Overshoot in these compounds can exist for many picoseconds leading to enhanced velocities over distances $\sim 1\ \mu m$. Although initial computations suggested that this velocity overshoot effect is less in InP than GaAs and that as a result InP would be expected to exceed GaAs in high frequency performance only for $L_g \gtrsim 1\ \mu m$, subsequent recalculations, including impurity scattering corresponding to a more reasonable doping level of $10^{17}\ cm^{-3}$ (cf. to zero in reference 95) and a more appropriate distribution of polar optic scattering angles in the central valley, led to the results shown in Figure 8 which are taken from reference 96. It can be seen that at all reasonable channel lengths, to the extent that the model is valid, the Monte Carlo calculation

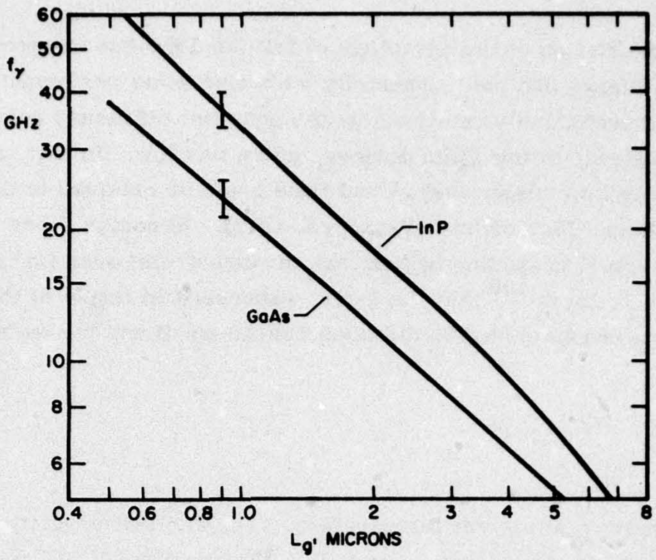

Figure 8. Response Frequency vs Gate Length for GaAs and InP (T.J. Maloney and J. Frey, IEEE Trans., ED-23, 519, 1976)

suggests that InP is indeed likely to perform in a superior fashion to GaAs at high frequencies. Hill, et al,[98] who have also reported on Monte Carlo calculations on these effects, also support this statement but they disagree with Maloney and Frey in details related to basic assumptions. Specifically they predict, in general, significantly higher cutoff frequencies for both InP and GaAs and a crossover in relative performance at a gate length of $\sim 0.4\ \mu m$ with GaAs being marginally preferred for smaller values.

A further consideration, elaborated by Shur[99] is that all the above calculations were made on the basis of an assumed uniform channel field. In practice, this is unlikely to be the case and as a result the maximum frequency of operation is likely to be reduced perhaps by as much as 30 percent below that predicted for a uniform channel.

However, high frequency characteristics are not the only determining factor. Another, and most important aspect of device performance is noise. It is this characteristic rather than higher efficiency or higher frequency capability that is currently generating most interest in InP for TED applications.

7.3 Device Noise

The early prediction of the advantage of InP for TED-use concerned its potentially higher efficiency and not necessarily its better noise performance. However, subsequent work presumably catalyzed by the potential efficiency gain led to the discovery that indeed, in InP Gunn devices, noise was low. In fact, it was found to be considerably lower than what at that time could be obtained in GaAs (for example, 7.5 dB vs 16.2 dB in GaAs at ~33 GHz). Kroemer[92] has summarized the early a posteriori reasoning behind this advance of InP over GaAs. To good approximation it is known[100] that the noise, expressed in terms of the "noise temperature" T_N is related to the diffusion coefficient D and the mobility μ of carriers by

$$T_N = K \cdot \frac{D}{\mu}$$

where K is a constant at a given temperature. The earliest predictions[2] simply suggested that both D and μ were large in InP thus making it ambiguous as to how this quotient might compare with GaAs. More recently[101, 102] it has been calculated that, because of the highly polar scattering in the primary minimum, above threshold in the region of intervalley scattering which is partially deterministic, the diffusion coefficient for electrons is low and should decrease further with increasing electric field. Of course this argument is also qualitatively applicable to GaAs as well. However, because of the higher threshold field in InP typical operating fields and thus the contribution of the partially ordered scattering compared to the random component are much increased. Subsequently it was shown[103] that if diffusion is taken into account in calculating the small signal impedance of a TED, then it is not possible to reach the D/μ limit given by the preceding equation. It is noteworthy, however, that the approach to this limit is closer in InP than in GaAs. Further complications[104] were shown to involve the $n\ell$ product in the TED as well as the cathode boundary conditions and doping uniformity.

Analytic consideration of even a couple of these effects soon becomes unwieldy. Sitch and Robson[100] attempted to circumvent this complexity by using a numerical solution for the noise in a transferred electron amplifier (TEA). From their calculations they concluded that the lowest noise that can be attained in either an InP or GaAs TEA is realized at a $n\ell$ product $\sim 3 \times 10^{10}$ cm^{-3}. In addition, it is desirable that the electric field should be essentially constant across the device with a value of 6 kV/cm in GaAs and 17 kV/cm in InP. To obtain such a flat field profile at low carrier density some kind of cathode barrier is required to limit injection, a conclusion in agreement with what is observed in InP in practice. The limiting noise measure they calculate is ~7 dB for GaAs and ~4.5 dB for InP; values they believe should be valid to as high as 50 GHz.

The fundamental reason behind this improved performance of InP is, as earlier suggested, its lower value of diffusion coefficient.[91]

When we consider the FET, however, things become less well understood. The fundamental noise limits on a transistor are in general set by different mechanisms than those prevailing in the TED.[105] As mentioned already, it is quite obvious that the static v/E curve appropriate to electrons in bulk material is just not applicable to transport in the thin layers of semiconductor employed in the FET. In fact, whether intervalley transfer occurs in the same sense in the FET as in the TED has not, to the authors' knowledge, been discussed. A summary of the current understanding of noise in the GaAs FET has been given by Lile.[106] As best as can be said at present, the noise limit in the GaAs metal semiconductor (MES) FET is set by thermal noise in the channel modified and amplified by the electrons drifting across the appreciable region of velocity-saturated carrier transport that exists in these devices. This diffusion noise is the dominant source of intrinsic noise in microwave GaAs FETs.[107]

It is the very low noise (typically 3 dB at 10 GHz in low noise devices) as well as its good high frequency performance that makes the GaAs MESFET such an attractive device. Despite the fact that the high field diffusion noise of the device is quite high, there is a strong correlation between the drain noise and the induced gate noise in this device. It is this correlation, which approaches unity and results in a cancellation between the two noise sources, which leads to the overall low net noise.[107]

We mentioned previously the lack of knowledge that exists at present concerning the dynamics of carriers in a FET structure. For GaAs it seems quite certain that velocity saturation does occur and, in fact, over probably quite a large fraction of the channel. Negative resistance effects are, however, suppressed. In the shortest channel devices, the fact of velocity saturation itself is somewhat difficult to reconcile; the transit time of the electrons in such devices is comparable with the relaxation time and as has been discussed earlier, this leads to the expectation of a continually increasing velocity. Himsworth[108, 109] concluded that the electric field in the channel of a junction field effect transistor (JFET) rose to a very high value only over a relatively limited distance and thus that electrons were travelling at unsaturated velocities over most of the source drain distance. However, the model used assumed a v/E relationship for the carriers appropriate to bulk material resulting also in the prediction of negative resistance for short gate devices. Whether this is appropriate in the case of the JFET is not known; it is believed not to be applicable to the MESFET as was discussed earlier and its inapplicability is substantiated by the lack of experimental observation of negative resistance in all but a few high power devices. Despite this, in GaAs the small signal and noise performance of these devices is consistent with velocity saturating.

When we turn to InP it becomes immediately apparent that little data or theoretical analysis exists on either the InP FET, in general, or on its noise performance in particular. Barrera and Archer[110] have reported on the results obtained with 1 μm gate length Schottky-gated devices fabricated on liquid phase epitaxial (LPE) layers of InP on Cr-doped InP substrates, and Frey[111] has analyzed the noise properties of InP vs GaAs FET devices using a Monte Carlo calculation. He concluded that whereas both InP and GaAs should exhibit very good low noise performance, the intrinsic InP devices should be slightly noisier than those made from GaAs at the same value of f/f_T. However, this difference may be somewhat nullified at any given frequency due to the fact that the current gain cutoff frequency, f_T, is higher for InP than for GaAs. At present, this is the only noise analysis that exists to the authors' knowledge for the InP FET. Although it is restricted by assumption to the below saturation region of operation of the device, Frey argues for the general applicability of this conclusion to more typical regions of operation. Although the relative merits of InP compared with GaAs regarding its noise performance and gain, etc., remain clouded for FET applications, there exists a considerable amount of interest in this material for application in this area. We shall return to this question in following sections where we shall consider, in detail, the relative technological importance of this semiconductor in the light of our present understanding.

7.4 Surface Properties

As we have already seen, the original reasoning for the advantages of InP for TED application subsequently were discounted. However, the argument did motivate work on both materials growth and the device technology and did result in devices which were indeed superior to GaAs, albeit in a different respect from that originally conceived (that is, noise vs efficiency). Ironically, a similar situation may be developing with regard to the FET. Following the TED developments, it was wondered whether the experimentally-observed lower noise of the TEDs might also be manifest in FETs made from this semiconductor. Subsequent work, although quite sparse at present, has failed to unambiguously decide this point; however, because the FET is a "surface controlled" device, this body of FET investigations did prompt a consideration of the surface properties of this material, a study which would have been quite incidental to the TED development. Although the data is at present limited, it is becoming apparent that in a certain sense the surface characteristics of InP are somewhat unique. It is the authors' opinion that whereas the InP FET may have few of the originally envisaged advantages over GaAs, it may nevertheless have attractive possibilities in this device area because of its superior surface characteristics.

The FET approach originally chosen with this material, and quite obviously so in light of the preceding experience with GaAs, was to use a metal for the gate control electrode. Such a MESFET Schottky-gate geometry has been highly successful on GaAs and technologically is, in principle, the simplest of all possible FET structures. However, whereas Schottky diodes may be readily fabricated on GaAs and ohmic contacts less easily so, the exact inverse obtains on InP. To date little success has been achieved in the fabrication of Schottky gates on InP[112] due to its low barrier height of ~ 0.45 eV compared to ~ 0.7 eV on GaAs. Attempts to improve this by annealing, the use of a thin intervening oxide layer between the metal and the semiconductor, and the use of exotic metal combinations have been tried. However, the reverse leakage remains relatively high (typically 5 mA at 3 to 4 V) and although reasoned otherwise by Barrera and Archer[110] would nevertheless seem to present limitations from the point of view of FET performance if in no other respect than in terms of reliability. The reasons for such a low barrier height on InP are largely unknown as are many other aspects of Schottky barriers in general. McCaldin, et al[113] have compiled the experimentally reported data on the III-V and II-VI compounds and observe an excellent correlation between the Schottky barrier height for holes with the electronegativity of the anion (P in the case of InP). However, such a wide spread in data exists due presumably to variations in preparation that it is to be expected that although a fundamental limit presumably exists on the barrier height on InP a large part of the data presently reported may be process-related.[114]

Prompted by both this limitation as well as certain postulated advantages for a metal insulator semiconductor-gated (MIS) FET in such applications as multigigabit logic[115] where the limitation of negative going only input levels requires signal inversion and level shifting between stages with the MESFET or reversion to slower low power designs, a modest amount of effort has been devoted to studies related to an insulated gate FET on InP.

MIS-capacitance/voltage studies have been performed on structures fabricated with both anodic[116,117] and pyrolytic[118] dielectrics on n-type InP which have in all cases suggested a very low value of $\lesssim 10^{11}$ cm^{-2} eV^{-1} for the apparent interface state density N_{SS} on the semiconductor. Although this value is at least one order of magnitude above that typically observed on the Si/SiO_2 system, it is more than an order of magnitude better than that reported by most workers for n-type GaAs. Interestingly, to a large extent the surface state results reported to date for both InP and GaAs seem to be almost independent of the dielectric employed[119-123] invariably indicating low state densities on InP and high values on GaAs. Although, at present, the only directly reported values for N_{SS} on InP have come from C/V measurements, there is some strong support for low surface trap densities from the work of Casey and Buehler.[124] These authors reported, from an analysis of

photoluminescence spectral intensities, that the surface recombination velocity on n-type InP is $\leq 10^3$ cm/sec compared to values of $\sim 10^7$ cm/sec observed for GaAs. Results on p-type InP were similar to those obtained on GaAs. Such low values of S on n-type material are quite consistent with the C/V data which suggests a low value of N_{SS} on this material. Additional evidence for the good surface properties of this semiconductor comes indirectly from photovoltage studies reported by Dahlberg[125] on (100)-oriented n-type material. These measurements showed that Ar-bombardment of the InP surface resulted in a very large change (>100 X) in the measured photo signal which was interpreted as being most likely due to enhanced surface recombination. Such a pronounced sensitivity to surface damage may suggest an initially low value for the rate of surface recombination on this material. However, we should note the earlier work of Barbarie and Fortin[82] on the quantum PEM effect in InP in which they concluded that their data was consistent with a large, and surface preparation dependent, value of S! Despite this, if these results allow for the above low state density interpretation, then the consequences for the device applications of this material are profound. Good interfacial characteristics would present, as it did for Si, the potential for integrated circuit (IC) applications of this material, something which is far less attractive for GaAs with its present limitation of a metal-gated technology active device.

Incidentally, it is perhaps not coincidental that whereas the surface state properties appear superior on InP to GaAs, the exact opposite applies with respect to Schottky diode performance.[126] To quote Casey and Buehler,[124] "The unique surface properties of InP are sufficiently different from other semiconductors that further work should be devoted to understanding surface states on InP as well as to applications that exploit this property." Although this is empirically most certainly the case, the reasons for it are unclear. Many attempts have been made in the past to relate actual surface state densities in "real" situations to those theoretically to be expected on a clean surface, but despite this very little understanding exists at present on real surfaces. What is known, primarily from photoemission studies on vacuum-cleaved samples, is that on Si, for example, whereas the Fermi level is pinned on the freshly-cleaved surface indicating a relatively large density of surface states, after exposure to as little as 10^3 langmuirs of oxygen, the pinning is largely removed.[127, 128] This apparent reduction of N_{SS} by oxygen exposure is at least consistent with the good interfacial characteristics exhibited by Si in contact with its thermal oxide. Conversely, for GaAs it is also known from photoemission studies that the surface pinning of vacuum-cleaved surfaces is aggrevated by the adsorption of oxygen.[78, 129] The effect of oxygen exposure on the surface photovoltage of real GaAs surfaces has been reported by Dahlberg.[130] Although some ambiguities remain,[131] this result is consistent with the large surface state densities invariably observed on GaAs for all presently

investigated dielectrics. (Note: Although many nonoxides such as Si_3N_4 have been investigated, in many cases it has been known that oxygen has been unintentionally incorporated into the layer and, in general, it is to be expected that some oxygen will be present.) For InP, however, this correlation does not evidently continue. Whereas the above reported data would suggest that the state density on real InP interfaces is small, the work of Chye, et al[132] perhaps suggests otherwise. These workers observed that photoelectron energy distribution curves were relatively insensitive to oxygen to exposures as high as 10^7 langmuirs. Beyond this level of oxygen, changes did result but were primarily due to the response of the O_2 itself, the Fermi level pinning remaining essentially unchanged. In contrast with this, it is perhaps of some relevance that in a comparison of GaSb, GaAs, and InP by photoemission studies on cleaved surfaces, Spicer, et al[133] conclude that more of the unfilled surface states, presumably associated with the As cation, lie within the forbidden gap in GaAs than in either of the other two semiconductors studied. Williams and McGovern[29] have also reported on a variety of measurements made on both vacuum-cleaved and real surfaces of InP. They observed from Kelvin probe surface photovoltage studies that exposure of a clean surface to the atmosphere leads both to a marked reduction in the photothreshold as well as to a large increase in yield. Although they interpret this as being due to an enhanced amount of band-bending and not necessarily to a reduction in the intrinsic state density, the data would not seem to preclude the latter interpretation. These authors also reported data, albeit with few details, on the saturation photovoltage of real surfaces, which showed a quiescent surface potential of ~ 80 mV for these etched (Br-methanol and 2 $HC\ell$ - 2 H_2O - HNO_3) surfaces.

8. DEVICE STATUS

The preceding sections have attempted to outline the reasoning and background information on InP and to present the arguments for the current interest in this semiconductor. When all this has been said, however, the question always reduces to that concerning the actual measured performance of devices. In this section, we will present results representative of the currently attainable levels of performance achieved in devices fabricated from InP and compare and contrast them with what can be accomplished with the more solidly established GaAs technology.

8.1 The Technology

The techniques and methods for device fabrication on InP are very similar to those employed on GaAs and Si. As with GaAs, recipes for ohmic contacts have been generated[134-136] with, once again, Au/Ge/Ni being suitable. However, as stated previously, the problem of forming good electrical contacts to InP is much less pronounced than is the case for GaAs.

Suitable etches are also well known with Bromine-Methanol being often quite satisfactory. Lubzens[137] reported a novel technique which employed a $FeCl_3$ solution as an etchant for n-type InP. In the dark this solution attacks InP very slowly; however, under illumination as a result of the light-induced change in surface potential, the etch-rate is much enhanced. As a result, fine patterns delineated optically may be etched. Stain etchants are available[138] for the delineation of epitaxial layers of this semiconductor which, in practice, present similar problems to those encountered in the GaAs technology and Huber and Linh[139] have reported on an etchant solution which effectively delineates defects.

The determination of carrier concentration profiles and via them the control of growth procedures to produce desired device structures presents a problem on InP. For GaAs the usual procedure is to employ a C/V measurement on either an Au- or Al-Schottky barrier. The leakage currents on such structures on InP are, however, so high as to invalidate the method at all but the lowest voltages. This can be overcome by cooling the structure;[140] however, from a practical point of view this is most certainly an inconvenience. Alternatively a C/V measurement on a MOS diode may be used.[141] This method, however, is far more time consuming and involves assumptions, for example, as to the role of the surface traps.

8.2 Transferred Electron Devices

We have seen in the preceding section how, because of its higher peak-to-valley ratio, the efficiency of InP TEDs is expected to be higher than that observed in GaAs. Moreover, the peak-to-valley ratio degrades less rapidly with increasing temperature which, combined with its higher thermal conductivity (0.35 W/cm^{o}C at 200^{o}C vs 0.46 W/cm^{o}C for GaAs), favors higher power CW operation for devices made from this semiconductor. This factor is significant because, as a result of its higher threshold field, high power levels are mandatory. In practice, the higher operating fields restrict CW operation of these devices to frequencies about $\sim$18 GHz where the active layer thicknesses are thin enough to allow adequate heat removal.

As an indication of the best that can presently be accomplished, we quote the results of the group at Varian.[140, 142] The InP used was grown by VPE in the thickness range 4 $\rightarrow$ 6 μm with doping levels from 0.5 to 5×10^{15} cm^{-3}. Contacts

were formed by growing a more low-doped region (cathode notch) with doping $\sim 10^{14}$ cm^{-3} which provides as uniform an electric field as possible. Such a uniform field is desirable for low noise operation so that as much of the device may be maintained in the optimum low noise field region of 15 to 20 kV/cm. At lower fields, near threshold, additional noise is generated by the random intervalley scattering of carriers between the primary and lowest subsidiary minima with the associated peak in the diffusion coefficient occurring in this region. At higher fields the mobility μ becomes small leading to enhanced noise through the D/μ dependence discussed earlier. Because of the high threshold field, heat sinking becomes a critical component of device design. A favored method and the one used by the group at Varian involves the use of an integral heat sink (IHS). Contacting to InP has been discussed by a number of authors.[134-136] It appears that the Au/Ge/Ni process used widely on GaAs also works satisfactorily on InP and was the process used on these devices.

Devices fabricated by the Varian group were designed for amplifier operation in the 26.5 to 40 GHz and 50 to 75 GHz ranges. Oscillator performance was, however, also evaluated. In general, the observation was made that the device Q of the InP devices was higher than that normally observed for GaAs viz. 7.7 vs 4.1 and that the InP devices appear to exhibit a far greater sensitivity of their negative resistance to bias voltage changes. InP devices from several wafers typically exhibited an 11 percent change for a 0.1V bias change compared to a 3 percent change on GaAs devices measured under the same conditions. The enhanced bias sensitivity, which was believed to perhaps be due to nonoptimum doping profiles, would indicate the requirement for more stringent control of power supply noise for these devices so as not to generate noise figure degradation in amplifier applications and higher AM conversion in oscillators.

Figure 9 is a compendium of the best reported oscillator results to date taken from reference 140. We might note the 200 mW operation with 4.6 percent efficiency at 23 GHz, 93 mW with 1.94 percent efficiency at 37 GHz, and significant power ($\leq$78 mW) with moderate efficiencies ($\leq$1.4 percent) throughout V-band (50 to 75 GHz).

For amplifier evaluation, circuits were designed to cover the lower half and upper half of the Ka band. Gains of $\lesssim$ 8 dB and 9 dB were observed respectively for these two ranges with noise figures in the low frequency circuit being in the range 13.0 to 15.8 dB. The lowest noise for this circuit was measured at 12.4 dB. High frequency circuit noise figures were in the 14.0 to 16.5 dB range. These compare very well with the 19 to 23 dB noise figures typically measured for similar GaAs devices at these frequencies.[143] Evaluation in the higher frequency range from 40 to 60 GHz demonstrated useful gain to frequencies as high as $\sim$47 GHz.

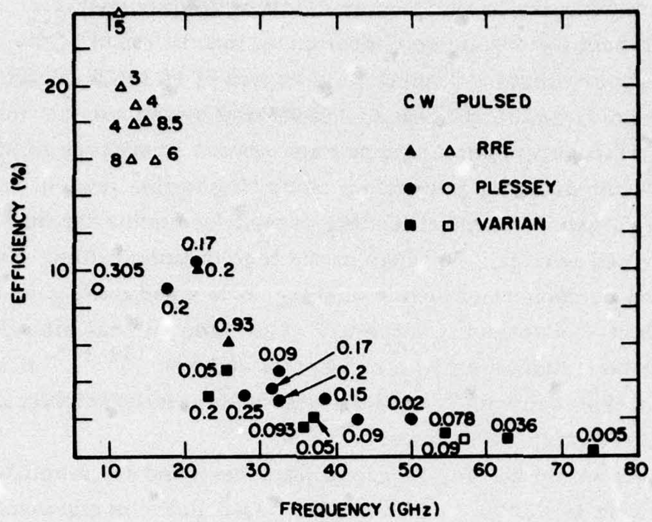

Figure 9. Summary to Date of Best Reported Oscillator Efficiencies as a Function of Frequency. Numbers associated with each datum correspond to output power in watts at that efficiency and frequency (R. J. Hamilton et al, IEEE Trans., MTT-24, 775, 1976)

A narrower band amplifier circuit was designed and built for the 18.0 to 26.5 GHz range. In this circuit, a noise figure of 10.1 dB with 9 dB associated gain was observed for these devices and represents the lowest reported InP noise figure in this frequency range to date.

From these results the conclusions were drawn that InP Gunn devices offer significant advantages over GaAs in both noise figure performance and as wide-band amplifiers. Noise figures of 13 dB less than that observed in GaAs have been observed with flat doping profile devices and 7 dB lower in the case of cathode-notched devices. These noise figures are also more than 7 dB less than what can be obtained with standard TWTs.

The results quoted above were all for devices operating in the "transit-time mode" where domains are generated at the cathode and then are propagated to the anode where they disappear. Such an operating mode, which is what was originally observed by Gunn, is invariably used for low power level devices.

When we consider high power applications, however, an alternative mode called "Limited Space Charge Accumulation" (LSA) becomes attractive. In this mode of operation, the buildup of space charge inhomogeneities (domains) is suppressed allowing access to the transferred electron bulk negative conductance of

the entire sample. The LSA element then acts as a true negative resistance whose frequency of operation, in contrast with the Gunn diode whose oscillation frequency is controlled by device length, is determined by circuit loading. Such devices, which can then be made from thicker material, have been made using GaAs which have shown very high peak powers of many hundreds of watts (pulsed) in X-band. The major disadvantage of such device operation is, however, the relatively low efficiency, 14 percent being about maximum for GaAs in X-band.

Mun, et al[144] have, they believe, unambiguously identified relaxation LSA mode operation of InP diodes fabricated from vapor-phase epitaxial material. These devices, operating in S- and X-band, have exhibited conversion efficiencies of, for example, 8.7 percent at 8 GHz with 16W of peak power. Such an efficiency, which is less than the value in excess of 20 percent which is to be theoretically expected in X-band for InP devices,[144] is no better than that obtainable from comparable samples in GaAs. It was anticipated by these workers that improvements in materials growth would lead to improvements in device efficiency. More recently[145] work has been reported on high power devices relying not on a true LSA mode of operation, but rather by inhibiting domain formation by the use of a current limiting cathode contact which acts to control hot-electron injection at the cathode and hence maintains a near uniform field distribution within the device. Using InP epitaxial layers of $\sim 34\ \mu m$ thickness efficiencies of 18 percent at 5 GHz have been observed with peak power $\sim 120W$.

In Europe the largest effort on InP Gunn devices is, not surprisingly considering their catalysis of this work, at the Royal Signals and Radar Establishment (RSRE, formerly RRE) and at Plessey. At the latter facility Gunn oscillators are being fabricated from VPE InP which exhibit 10 watt pulsed at 15 GHz with 15 percent efficiency. Amplifiers using similar devices with a 100Å doping spike located 3 μm below the epitaxial layer surface have shown small signal gains of 8.5 dB over the 12 to 18 GHz frequency range with 10 dB gain when tuned for narrow band operation.

As has been stated earlier, apart from Si, the only other semiconductor which at present is used in any commercially available solid-state device is GaAs. Specifically, no devices made from InP are at present commercially available. However, developments at a number of industrial facilities have reached the stage where an objective evaluation would suggest that InP Gunn devices may well be very close to commercial exploitation.

8.3 Field-Effect Transistors

As was stated previously, it was the Gunn device that was originally expected to benefit from the use of InP. Subsequently, efforts were undertaken to determine whether improved performance might not also be obtained in FET applications. Although the amount of work in this area reported to date is limited, some conclusions have been drawn. Thus, it is probably representative to say that most workers feel that more data must be obtained before a definitive statement may be made on whether InP offers decided advantage over GaAs in this area of application.

The earliest reported work in this area was that of Barrera and Archer,[110] who reported on the characteristics of 1 μm gate MESFETs fabricated on LPE layers of InP grown on 10^4 Ω-cm Cr-doped InP substrates. These layers had electron concentrations in the range of 5×10^{16} to 2×10^{17} cm^{-3} and mobilities at room temperature $\lesssim 4000$ cm^2/V-sec. Alloyed Au/Ge was used for the source/drain contacts and Cr-Au for the gate.

Such devices, fabricated using the same device geometry and photolithographic procedures that have become standard for GaAs FETs, were characterized as to both their low frequency and their microwave performance. Good saturating output characteristics were obtained which were essentially free from looping. However, due perhaps to either the relatively low resistivity substrate or thermal degradation at the epilayer/substrate interface, it was not possible to completely pinch off the channel. Direct current transconductance values were observed to be higher for these devices than is typically observed for GaAs and to increase with doping level. Values for g_m of 100 mmhos for $n = 1.4 \times 10^{17}$ cm^{-3} and 50 mmhos has for $n = 6 \times 10^{16}$ cm^{-3} being representative. The ratio of g_m for InP devices to that for GaAs was ~ 1.4 which agrees well with that theoretically expected due to the difference in saturation velocity. Table 9 summarized the results obtained by these workers for both InP and GaAs devices of the same geometry. It can be seen that whereas the current gain cutoff frequency is higher for InP in other respects, the GaAs devices are marginally better. In particular, the lower noise benefit obtained with InP in TED applications was not evident here. In considering the results shown in Table 9, however, it should be remembered that although the epilayers used by Barrera and Archer were very good, the stage of development of this semiconductor is far behind that of GaAs and so the results they quote should be viewed only as what can be presently accomplished.

Although the quality of their Schottky gates was no better than that generally reported by other workers, Barrera and Archer surprisingly felt that this did not limit the microwave performance of their devices.

Table 9. Comparison of the Properties of Identical Structure InP and GaAs MESFETs Fabricated by Hewlett-Packard Laboratories (taken from reference 110)

Parameter	Inp		GaAs	
	$n = 6\times10^{16}cm^{-3}$	$n = 1\times10^{17}cm^{-3}$	$n = 6\times10^{16}cm^{-3}$	$n = 1\times10^{17}cm^{-3}$
Current gain cutoff frequency (f_T), GHz	20	20-24	11	13
Mason's unilateral power gain cutoff frequency (f_{max}), GHz	33	32	40	40
Maximum available gain at 10 GHz (MAG), dB	7.9	7.8	11	11
Noise figure for MAG at 10 GHz, dB	6.0	9.5	7.5	6.2
Minimum noise figure at 10 GHz, dB	4.8	6.0	3.5	3.2
Associated gain at 10 GHz, dB	5.8	5.5	6.6	7.8
Transconductance (g_{m_o}), mmho	50	84	33	53

Their results were fitted to an equivalent circuit from which they deduced values for the transistor elements. In particular, they found for the InP device, a much larger value (~ 5X larger) of gate-to-drain capacitance than that which exists in the GaAs transistor and also a far smaller value of gate-to-drain resistance. Both of these differences would result in an increased degenerative feedback in the InP device resulting in the observed loss in power gain shown in Table 9. It was not apparent from this study whether the difference between the InP and the GaAs was intrinsic to the material or was a result of some deficiency in device structure or material quality. It was calculated that if the values of the gate-to-drain capacitance and the drain-to-source resistance, which was also less in the InP case, could be increased to values approaching those observed with GaAs then f_{max}, for example, would be increased from its presently measured value of 32 GHz to 79 GHz, a value well in excess of anything possible with GaAs. Similar significant improvements in power gain would also ensue.

The above work, representing the only published work to date on the InP MESFET thus indicates that at present, although the InP device shows improved current gain, its power gain and noise figure are inferior to that which can be achieved with GaAs. As admitted by Barrera and Archer, however, improvements in the quality of the InP might well remedy this situation.

Ion implantation experiments in InP are being conducted at Westinghouse Corp., Lincoln Laboratories, Naval Research Laboratory and RADC/ET. The Westinghouse program is a study effort, the Lincoln program is aimed at IMPATTs and similar structures, and the RADC/ET program is directed toward the determination of optimum implant and annealing conditions for both n and p type dopants. The NRL program is for FETs and consists of Si implants into Fe doped InP. The Si doping is performed to get an "n" layer with a carrier concentration of about 6×10^{16} to $4 \times 10^{17}/cm^3$. Implantation is carried out at 170K volts, then after capping with silicon oxy nitrite followed by 5 percent P doped SiO_2 an activation anneal is run for 15 minutes at $700^{\circ}C$ with about 20 to 30 percent activation. Using Au Schottky gates (gate width 2 μm) and Au-Ge ohmic contacts, FETs have been prepared having 13.7 dB gain at 8 GHz and 11.1 dB gain at 10 GHz, pinch off is at 2 volts. At this point, the processing including contacts is not optimum; however, the work appears promising. Using an MIS structure FET, where the gate is pyrolytic SiO_2, the Naval Ocean System Center has made a 4 μm gate FET with 14 dB gain at 1 GHz. The InP layer was prepared by LPE using an etch back technique.

9. CONCLUSIONS

The preceding report represents, to the authors' best knowledge, a comprehensive and exhaustive summary of the present state of our understanding and the present stage of development of InP. It is apparent from what has been said that at the same time that InP is of considerable technological interest, it is also at a relatively immature stage of deveopment. This is not meant to imply that commercial application in the near future is unlikely. To the contrary, InP Gunn devices would seem near commercial exploitation. What it does mean is that before routine use of this semiconductor can be envisaged in such applications as FETs, a considerable amount of further materials development must be forthcoming. Of all of the preceding, it is the unique surface properties of this semiconductor which should seem to date to have received a disproportionately small share of the research interest. In the authors' opinion it is this fact, of good surface properties, that promises much technological payoff in such areas as microwave integrated circuits. To date, such an application for any of the III-Vs

has received much attention but little practical effort. Exceptions exist such as is represented by the MESFET IC work at Hewlett-Packard, but compared to silicon this is a very small effort.

The material effort to date has not been sufficient to determine what are the material shortcomings in relation to device parameters. Adequate amounts of semiinsulating substrates have not been available for device studies. The amount and quality of epitaxial InP for device fabrication has not been adequate to determine types of contacts, preparation of Schottky barriers, surface passification, etcetera. Thus, there are many unanswered questions on InP materials which will have to be addressed prior to answering the question, "what device limitations are due to material problems?"

It should be mentioned in conclusion that because of space limitations a conscious effort has been made to restrict this discussion to InP and to exclude all references to related ternary and quaternary compounds. This should not be taken to infer that these other materials are of lesser interest or importance. In fact, semiconductors such as InAsP and GaInAsP have tremendous technological potential and may well overshadow InP in the final analysis as to what makes the "best" device.

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